Application No. 09/252,551

IN THE CLAIMS

Please amend Claims 134, and 142-144 as set forth below in reissue amendment format:

105
134. (Amended) A bidirectional data communication system 104 according to claim 133, wherein the first timing loop includes a high gain error generator, a loop filter, and an oscillator circuit, the high gain error generator responsive to characteristic values of the timing signals, and wherein the second timing loop includes a low gain error generator, a loop filter, and an oscillator circuit, the high gain error generator responsive to characteristic values of the data signals.

108
142. (Amended) A bidirectional data communication system 107 according to claim 141, the receiver block further comprising timing recovery circuitry coupled to receive the digital signal from the analog to digital converter and extract timing information therefrom, the analog to digital converter operatively responsive to said timing information and performing digital conversions at a rate defined thereby.

109
143. (Amended) A bidirectional data communication system 108 according to claim 142, wherein the timing recovery circuitry comprises a first timing loop having a high gain stage and a second timing loop having a low gain stage, the first timing loop locking the analog to digital converter in phase with the preamble portion the second timing loop locking the analog to digital converter in phase with the data containing portion.

110
144. (Amended) A bidirectional data communication system 109 according to claim 143, wherein the first timing loop includes a

47